IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A frame synchronizing device for a binary data transmission system wherein digital data are transmitted as a serial bit stream organized into frames, each frame including a pre-defined frameheader, comprising:

a serial input parallel output shift register means for receiving said serial bit stream and outputting said frames in a consecutive order, said shift register means including a serial input portion and a parallel output portion and having at least as many stages as the number of bits of a frame,

characterized by controlling means for detecting whether or not a frameheader is present at the output of said parallel output portion and, if not, controlling said shift register means so that the outputting of a frame from said parallel output portion is delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one, until synchronization is reached.

2. (Original) The device according to claim 1, wherein said controlling means is adapted so that the delay of the outputting of a frame is repeated several times until synchronization is reached.

3. (Currently Amended) The device according to claim 1 ~~or 2~~, wherein the frames have a fixed length.

4. (Original) The device according to claim 3, wherein the frames are bytes.

5. (Currently Amended) The device according to claim 1~~at least any one of the preceding claims~~, comprising
a first clock means for generating first clock pulses clocking said parallel output portion of said shift register means, wherein controlling means are adapted to control said first clock means so that said first clock pulses are delayed by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one.

6. (Original) The device according to claim 5, wherein each frame includes N bits, a second clock means is provided for generating second clock pulses for clocking said serial input portion of said shift register means, and said first clock means converts said second clock pulses into said first clock pulses having a time period which is N times longer than the time period of said second clock pulses, characterized in that said controlling means is adapted to control said first clock means so that said first clock pulses are delayed by at least one time period of said second clock pulses.

7. (Currently Amended) The device according to claim 5~~or 6~~, wherein said controlling means is adapted to supply a ("kick-pin") control signal to said first clock means, and said first clock means is adapted so that it is blocked by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one.

8. (Original) A frame synchronizing method for a binary data transmission system wherein digital data are transmitted as a

serial bit stream organized into frames, each frame including a pre-defined frameheader, comprising the steps of:

inputting said serial bit stream into a serial input portion of a serial input parallel output shift register means having at least as many stages as the number of bits of a frame, and outputting said frames in a consecutive order from a parallel output portion of said shift register means, characterized by the further steps of:

- detecting whether or not a frameheader is present in the output of said parallel output portion, and,

- if not, delaying the outputting of a frame from said parallel output portion by at least one time period which is needed for shifting a bit in said serial input portion from a stage to a next one, until synchronization is reached.

9. (Original) The method according to claim 8, wherein the step of delaying the outputting of a frame is repeated several times until synchronization is reached.

10. (Currently Amended) The method according to claim 8~~ or 9~~, wherein the frames have a fixed length.

11. (Original) The method according to claim 10, wherein the frames are bytes.

12. (Currently Amended) The method according to claim 8~~at least any one of claims 8 to 11~~, comprising the further step of generating first clock pulses clocking the outputting of the frames from said parallel output portion of said shift register means, characterized in that said first clock pulses are delayed by at least one time

period which is needed for shifting a bit in said serial input portion from a stage to a next one.

13. (Original) The method according to claim 12, comprising the further steps of:

generating second clock pulses for clocking the inputting of said serial bit stream into said serial input portion of said shift register means, and

converting said second clock pulses into said first clock pulses having a time period which is N times longer than the time period of said second clock pulses, wherein each frame includes N bits, characterized in that said first clock pulses are delayed by at least one time period of said second clock pulses.

14. (Currently Amended) The method according to claim 12~~ or 13~~, characterized by the further steps of:

generating a ("kick-pin") control signal, if a frameheader is not detected in the output of said parallel output portion of said shift register means, and

blocking the generation of said first clock pulses by said control signal for at least one time period which is needed for shifting a bit in said serial input portion of said shift register means from a stage to a next one.

15. (Currently Amended) A digital data transmission systems like SONET/SDH or Gigabit Ethernet comprising a device as claimed in Claim 1 ~~or working using a method as claimed in Claim 8~~ where serial data are transported over a single channel and, at the receiving side, is converted into parallel data for further processing.